

JEDEC PUBLICATION

2.5D/3D Silicon Thinned Wafers with Through Silicon Vias (TSVs) and Backside Redistribution Layer (RDL): Reliability Guidelines Relative to the Underlying 2D CMOS Technology

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**2.5D/3D SILICON THINNED WAFERS WITH THROUGH SILICON VIAS (TSVS) AND
BACKSIDE REDISTRIBUTION LAYER (RDL): RELIABILITY GUIDELINES RELATIVE
TO THE UNDERLYING 2D CMOS TECHNOLOGY**

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Introduction

To meet the required increase in IC device bandwidth, reduced power and form factor shrinks, semiconductor manufacturers are implementing two-point five (2.5D) interposer and three-dimensional (2.5D/3D) chip stacking using Copper Through Silicon Vias (Cu-TSVs). Future revision may include TSV materials other than Cu but are considered out of scope for this revision. Key manufacturing deliverables to allow this 2.5D/3D integration are 2D silicon thinned wafers with Cu-TSVs and Backside Redistribution Layers (RDL). The introduction of these key 2.5D/3D process elements in a qualified 2D CMOS silicon technology leads to new reliability challenges and requirements with respect to the adopted 2D technology.

The intent of this publication is to provide silicon manufacturers with the minimal amount of reliability characterization needed to send 2D thinned wafers with Cu-TSVs and RDL processing to their customers. It is not meant to be a comprehensive document, as additional tests may be required based upon specific process/package requirements not covered here. Full 2.5D/3D reliability qualification should come from an agreement between the customer and the supplier.

2.5D/3D SILICON THINNED WAFERS WITH THROUGH SILICON VIAS (TSVS) AND BACKSIDE REDISTRIBUTION LAYER (RDL): RELIABILITY GUIDELINES RELATIVE TO THE UNDERLYING 2D CMOS TECHNOLOGY

(From JEDEC Board Ballot JCB-25-79, formulated under the cognizance of the JC-14.2 Subcommittee on Wafer-Level Reliability.)

1 Scope

Key process elements of 2.5D/3D chip stacking technologies are Copper Through Silicon Vias (Cu-TSVs) with wafer thinning followed by a Backside Redistribution Layer (RDL) process. The intent of this publication is to provide guidelines for a minimal reliability characterization of 2.5D/3D processed thinned wafers with Cu-TSVs and Backside RDL. These guidelines only apply to Cu-TSVs and do not apply to any other TSV metallization. These guidelines include the characterization of thinned wafers with the TSV via first, middle, or last process.

The reader is referred to JEP158 for guidelines on Multiple Bonded Wafers characterization.

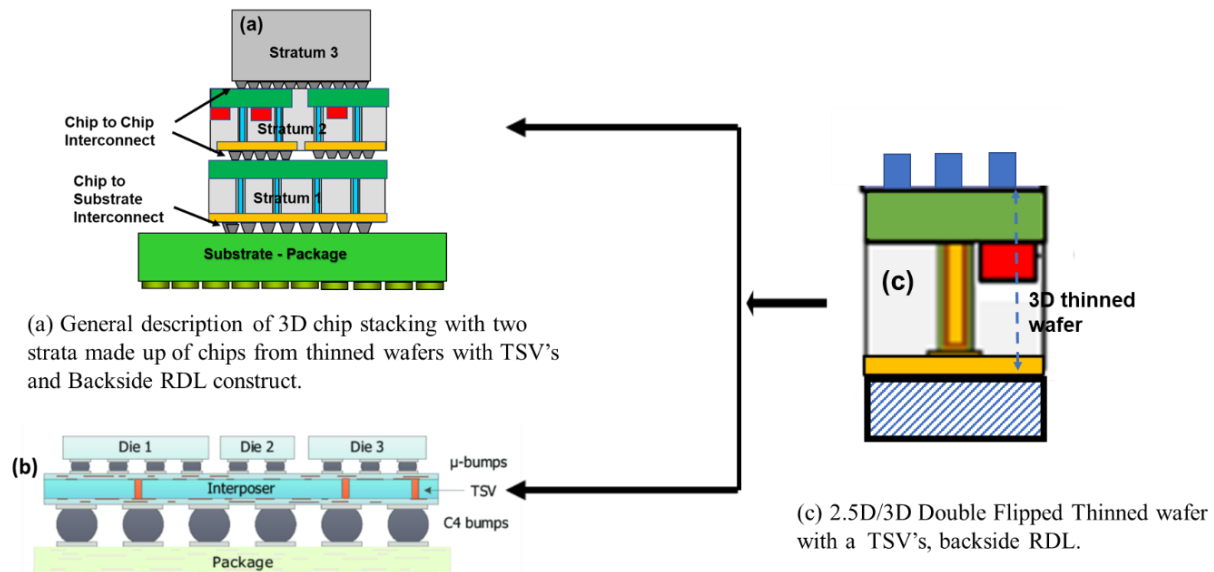
This publication is limited to the introduction of the 2.5D/3D process elements applied to a fully qualified 2D CMOS technology. This includes standard planar MOSFET, FinFET and future CMOS technologies. In addition, the scope is limited to TSV introduction in Silicon Bulk Technologies.

The 2.5D/3D reliability characterization is focused on quantifying:

- The delta between the 2D thick and the 2.5D/3D thinned wafers with respect to the 2D CMOS FEOL/MOL/BEOL intrinsic wear mechanisms.
- The intrinsic reliability wear-out mechanisms associated with the introduction of TSVs, the Backside RDL and wafer thinning.

Figure 1 describes the typical DUT part of a 2.5D/3D thinned wafer in which this publication is giving key reliability guidelines. This thinned wafer is associated with either 3D (a) or 2.5D (b) packaging. This DUT is part of a 2.5D/3D double flipped process (c) described further in Figure 2. This double flipped process allows the DUT to be tested using BEOL pads as was done for 2D thick wafers (see Figure 2 (d)). It is expected that the double flipped process will not impact the reliability of the 2.5D/3D thinned wafer delivered to the customer.

1 Scope (cont'd)



(b) General description of 2.5D chip stacking with interposer made up from thinned wafers with TSV's and Backside RDL elements.

(a) Example of 3D chip stacking with TSVs and interconnections between strata in the stack. Stratum 1 and Stratum 2 are examples of thinned chips with TSVs and Backside RDL construct, respectively, with and without active devices (MOSFETs).

(b) Example of 2.5D interposer packaging with TSV and Backside RDL.

(c) Typical DUT from a 2.5D/3D double flipped thinned wafer this publication is recommending using to evaluate key reliability guidelines.

Figure 1 — Example of 2.5D/3D Chip Stacking

Most of the recommended reliability evaluation is based on Wafer Level Reliability (WLR) testing, but, when needed, the use of module (proxy package) level stressing is recommended as part of the 2.5D/3D reliability evaluation. These tests are performed on a combination of 2D thick wafers, 2.5D/3D thick wafers, and 2.5D/3D thinned wafers depending on the reliability mechanism to be evaluated. The selected wafers for this testing are 2D wafers and 2.5D/3D wafers manufactured with the process of record adopted for 2.5D/3D product. In addition, guidelines on recommended structures to be used for the 2.5D/3D WLR evaluation are provided.

1 Scope (cont'd)

This publication assumes:

- 1) 2D Technology Qualification.
 - a. It is assumed that it has been completed prior to the addition of 2.5D/3D elements and that it is manufacturable.
- 2) 2.5D/3D Elements introduced into the 2D technology covered in this publication.
 - a. Copper Through Silicon Vias
 - b. Wafer Thinning
 - c. Backside Redistribution Layer Process

This publication covers the minimum guidelines on the following 2.5D/3D reliability qualification items:

- 1) Requalification of the 2D FEOL/MOL/BEOL reliability elements (Intrinsic wear out mechanisms, defect density) with the added 2.5D/3D elements.
 - a. Using the same stress and test methodology originally done on the already qualified 2D CMOS processes.
- 2) Additional reliability testing needed on the 2D CMOS elements due to added 2.5D/3D Elements.
 - a. Clause 5.
 - i. TSV Mechanical Proximity Effects.
 - ii. Global Effects (2.5D/3D effects to 2.0D CMOS technology in addition to mechanical proximity effects).
 - iii. Plasma Induced Damage (Possible PID damage to 2D FEOL due to introduction of the 2.5D/3D elements into the 2D CMOS process).
 - b. Clause 8 – Impact of Stress Migration and Thermal Cycling to 2D BEOL reliability due to the introduction of the 2.5D/3D elements.
 - c. Clause 9 – Impact of SM/HTS and Thermal Cycling to the 2D FEOL/MOL reliability due to the 2.5D/3D elements.
- 3) 2.5D/3D key reliability Qualifications elements.
 - a. Clause 6 – Cu-TSV Electromigration (EM).
 - b. Clause 7 – Cu-TSV (Dielectric/Metallic Liner) , TSV/RDL and TSV/Mx interface integrity.
 - c. Clause 9 – Impact of SM/HTS and TC on Cu TSV, TSV/RDL & TSV/Mx interface integrity.

This publication does not cover any additional processing after wafer thinning (bumps, 2.5D/3D packaging, etc.) and is not meant to be a comprehensive document, as additional tests may be required based upon specific process/package requirements not covered here. Full qualification should come from an agreement between the customer and the supplier.

2 Terms and Definitions

2D CMOS process: Manufacturing process associated with a 2D CMOS technology using thick wafers with no TSV and RDL layer (See Figure 3.a).

2.5D packaging: In 2.5D packaging scheme, two or more active semiconductor chips are placed side-by-side on a silicon interposer for achieving extremely high die-to-die interconnect density.

3D packaging: In 3D structure, active chips are integrated by die stacking for shortest interconnect and smallest package footprint.

2.5D & 3D process: Manufacturing process associated with a 2.5D/3D packaging technology using thinned 2D wafers with TSVs and Backside RDL layers with/out active devices (MOSFETs, Capacitors, Resistors, etc.).

back end of line (BEOL) (adj): Pertaining to the last portion of the semiconductor IC processing that creates the conductive lines carrying power and signals between devices and to the interface connecting off-chip.

back end of line (BEOL) (noun): The last portion of the semiconductor IC processing that creates the conductive lines carrying power and signals between devices and to the interface connecting off-chip.

BTI: Bias Temperature Instability is a time, temperature and electric field dependent device degradation mechanism encountered in metal-oxide-semiconductor (MOS) field effect devices that can cause a drift in device parameters such as the threshold voltage V_{th} .

CHC: Channel Hot Carrier is a device degradation mechanism caused by channel impact ionization during saturated conduction at high V_{ds} .

Cu pumping: the irreversible extrusion of Cu from Cu-filled through-silicon vias (TSVs) exposed to high temperatures during back-end of line (BEOL) processing.

CVS: Constant Voltage Stress

double flipped thinned wafer process: Process where the 2.5D/3D thinned wafer is attached to a carrier on the RDL back side and the wafer thinning carrier is removed (See Figure 2). This allows for reliability testing with probe pads from the BEOL side.

device under test (DUT): A device that is tested to determine performance, proficiency and reliability. A DUT also may be a component of a bigger module or unit.

electromigration (EM): BEOL reliability wear out mechanism associated to the movement of atoms due to the flow of current through a BEOL metal layer. If the current density is high enough, the heat dissipated within the material will repeatedly break atoms from the structure and move them. This will create both 'vacancies' and 'deposits'.

failure analysis (FA): The physical, chemical, electrical, or other process that has led to a nonconformance.

2 Terms and Definitions (cont'd)

NOTE A failure mechanism may be characterized by how a degradation process proceeds including the driving force (e.g., oxidation, diffusion, electric field, current density).

failure mode (general): The way in which a failure mechanism manifests itself in a failing component.

front end of line (FEOL) (adj): Pertaining to the first portion of the semiconductor IC processing that creates active devices such as transistors, capacitors, diodes, etc. For MOSFET devices the FEOL ends with the gate conductor formation.

front end of line (FEOL) (noun): The first portion of the semiconductor IC processing that creates active devices such as transistors, capacitors, diodes, etc. For MOSFET devices the FEOL ends with the gate conductor formation.

HTS: High Temperature Storage test is typically used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms of solid-state electronic devices.

KOZ: Keep Out Zone.

I_{stress} : Applied stress current.

middle-end-of-line (MOL) (adj): Pertaining to the middle portion of the semiconductor IC processing that builds the connection between FEOL (Gate, Source and Drain diffusions) and BEOL (first metal).

middle-end-of-line (MOL) (noun): The middle portion of the semiconductor IC processing that builds the connection between FEOL (Gate, Source and Drain diffusions) and BEOL (first metal).

module level stress (MLS): Stress of selected 2.5D/3D DUTs that are part of a double flipped thinned wafer with pads wire bonded to a proxy package.

plasma induced damage (PID): MOSFET devices damage due to bombardment of high-energy ions and plasma stressing during plasma etching as part of BEOL, TSV and RDL processing. The amount of damage that is tolerable is defined by the Design Manual Antenna rules.

stress migration (SM): Stress migration is a mass transport intrinsic wear out mechanism that may occur in the BEOL metal lines or vias. When stress migration occurs, stress gradients provide the driving force for the accumulation of vacancies.

Gate Dielectric TDDDB: Time-Dependent Dielectric Breakdown is a CMOS oxide degradation due to e-field and oxide tunneling that leads to oxide shorts from gate-to-channel.

temperature cycle/thermal cycling (TC): Temperature Cycling or Thermal Cycle testing is performed on materials to determine the resistance of exposure to alternating extremes of high and low temperatures. It is an environmental stress test used in evaluating product reliability as well as in manufacturing to catch early-term, latent defects by inducing failure through thermal fatigue.

T_{stress} : Applied temperature at stress

t_{stress} : Time under applied stress condition.

2 Terms and Definitions (cont'd)

through silicon via (TSV): TSVs are vertical wires used to precisely connect stacked chips. They are formed by etching trenches into silicon and then filling them with insulating liners and metal wires (Cu, Al, Poly-Si).

TSV via-first: A TSV formed before completion of the silicon device fabrication (FEOL).

NOTE These vias may be created before or during front-end-of-line (FEOL) but before back-end-of-line (BEOL) processing. They are created by etching them from the top side of the wafer and are buried below the subsequent BEOL layers. The process allows for interconnects with a high density. These vias connect circuits at the global or intermediate IC level.

TSV via-middle: A TSV formed after FEOL processing and prior to or during the BEOL process.

NOTE A “via-middle” process is sometimes considered to be part of a “via-first” process.

TSV via-last: A TSV formed after the completion of the silicon device fabrication, specifically after the completion of both FEOL and BEOL layer processes.

NOTE TSVs connect circuits at the bond-pad level.

voltage ramp stress (VRS): Voltage Ramp Stress consists of an applied voltage waveform to a DUT terminal that increases or decrease as function of time. It is typically characterized by a constant rate of change, or slope, and is often used in electronic circuits for testing and measurement purposes.

wafer thinning: Process of wafer manufacturing associated to the removal of silicon from the back side of a 2.5D/3D thick wafer to a desired thickness. The two most common methods of wafer thinning are conventional grind and chemical-mechanical planarization (CMP).

wafer level reliability (WLR):

The process of evaluating the reliability of semiconductor devices or IC products while they are still part of a wafer.

3 Normative References

The following normative documents contain provisions that, through reference in this text, constitute provisions of this publication. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this publication are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies. Informative documents are listed in the annex entitled “Bibliography”.

2.5D/3D

JEP158, *3D Chip Stack with Through-Silicon Vias (TSVs): Identifying, Evaluating and Understanding Reliability Interactions*.

TDDb

JESD263, *Gate Dielectric Breakdown*.

JEP159A, *Procedure for the Evaluation of Low-k/Metal Inter/Intra-level Dielectric Integrity*.

3 Normative References (cont'd)

Electromigration

JESD61A, *Isothermal Electromigration Test Procedure.*

JESD63, *Standard Method for Calculating the Electromigration Model Parameters for Current Density and Temperature.*

JESD202, *Method for Characterizing the Electromigration Failure Time Distribution of Interconnects under Constant-Current and Temperature Stress.*

JESD33B, *Standard Method for Measuring and Using the Temperature Coefficient of Resistance to Determine the Temperature of a Metallization Line.*

JEP001-1A, *Foundry Process Qualification Guidelines – Backend of Line (Wafer Fabrication Manufacturing Sites)*

Hot Carrier

JESD28-A, *A Procedure for Measuring N-Channel MOSFET Hot-Carrier-induced Degradation at Maximum Gate Current Under DC Stress.*

JESD60A, *A Procedure for Measuring P-Channel MOSFET Hot-Carrier-induced Degradation at Maximum Gate Current Under DC Stress.*

Bias Temperature Instabilities

JESD241, *Procedure for Wafer-Level DC Characterization of Bias Temperature Instabilities*

JEP001-2A, *Foundry Process Qualification Guidelines – Front End Transistor Level (Wafer Fabrication Manufacturing Sites)*

Stress Migration

JEP139, *Guideline for Constant Temperature Aging to Characterize Aluminum Interconnect Metallizations for Stress-induced Voiding.*

JESD214, *Constant-Temperature Aging Method to Characterize Copper Interconnect Metallizations for Stress-induced Voiding*

Temperature Cycling

JESD22-A104F.01, *Temperature Cycling*

JESD47L, *Stress-test-driven Qualification of Integrated Circuits*

Wafer Level Temperature Storage

JESD22-A103E.01, *High Temperature Storage Life*

4 Expected 2.5D/3D WLR Coverage by Mechanism

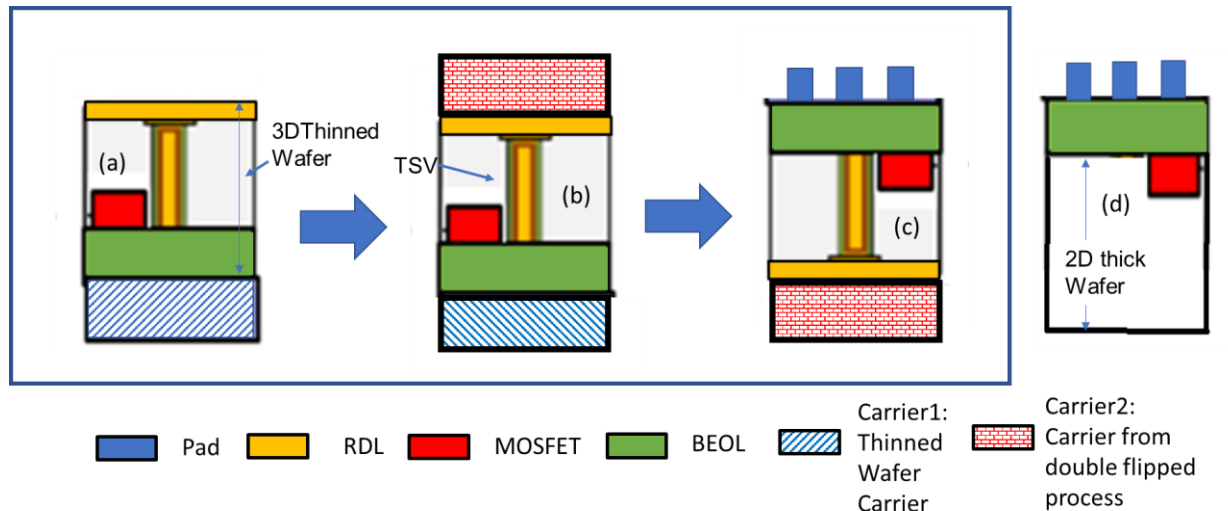
Table 1 gives the list of the Reliability wear-out mechanisms covered in this publication for TSV/wafer thinning/RDL process introduction. It is assumed that the underlying 2D silicon technology is a fully qualified CMOS technology. Details of each recommended testing procedure are provided in the following paragraphs.

Table 1— Key Reliability Activities to Evaluate the Impact of 2.5D/3D Wafer Thinning with TSV and Backside RDL to an Underlying 2D CMOS Qualified Technology

2.5D/3D Mechanisms	Failure Risk	Wear-out mechanism test methods covered in this publication	
TSV Cu pumping	BEOL Failure	SM, TC	Clauses 8, 9
		2D BEOL Reliability testing in 2.5D/3D wafer	Clause 5
Effects on the underlining 2D technology of TSV, Wafer thinning, RDL processes	TSV induced delamination	SM, TC	Clauses 8, 9
	<ul style="list-style-type: none"> • TSV mechanical proximity effects • Global effects 	2D Reliability testing in 2.5D/3D thinned wafers.	Clause 5
TSV Barrier/Liner roughness, non-uniformity.	Liner Breakdown (Leakage/short)	VRS	Clause 7
	Cu diffusion	<ul style="list-style-type: none"> • This topic is not part of this document. • It is recommended to be part of the product level High Temperature Storage stressing/testing (HTS) included in the package level qualification. TSV Cu diffusion induced leakage and Reliability impact to FEOL could manifest during HTS. Proper Failure Analysis (FA) could confirm Cu diffusion in the FEOL devices. 	
Voids in TSV	Corrosion, Effects EM, Liner integrity	SM, TC, EM, VRS	Clauses 5, 6, 7, 8, 9
TSV Electromigration	Open, High R	EM	Clause 6
TSV/RDL Plasma Induced Damage	Device impact	2D FEOL Reliability testing in 2.5D/3D thinned wafers	Clause 5

4.1 Stress and Test Vehicles

The recommended test vehicle is a double flipped 2.5D/3D thinned wafer. Figure 2 gives an example using the Cu-TSV via first process. This test configuration allows the running of reliability tests similarly to what was done previously for 2D thick wafers. In this case, testing pads are connected to the Device Under Test (DUT) through BEOL wiring and allow the DUT to be tested. It is expected that the double flipped thinned wafer (Figure.2 (c)) will have the same reliability as thinned wafers coming from the manufacturer (Figure 2 (a)).



Example of double flipped (c) thinned wafer with a Cu-TSV via first process with the Backside RDL. The double flipped thinned wafers originate from the manufacturer as thinned wafers with Backside RDL (a) on top of a carrier (carrier1). These thinned wafers are flipped once a second carrier (carrier2) is attached (b).

- (a) 3D thinned wafer with carrier needed for the thinning process as delivered to the customer.
- (b) Intermediate step of 3D thinned wafer (a) with carrier attached to the RDL metal part of the double flipped process.
- (c) Final step of the double flipped process where the thinned wafer carrier is removed from (b) and pads are connected through the BEOL to the active devices.
- (d) 2D thick wafer with same BEOL and FEOL as (c).

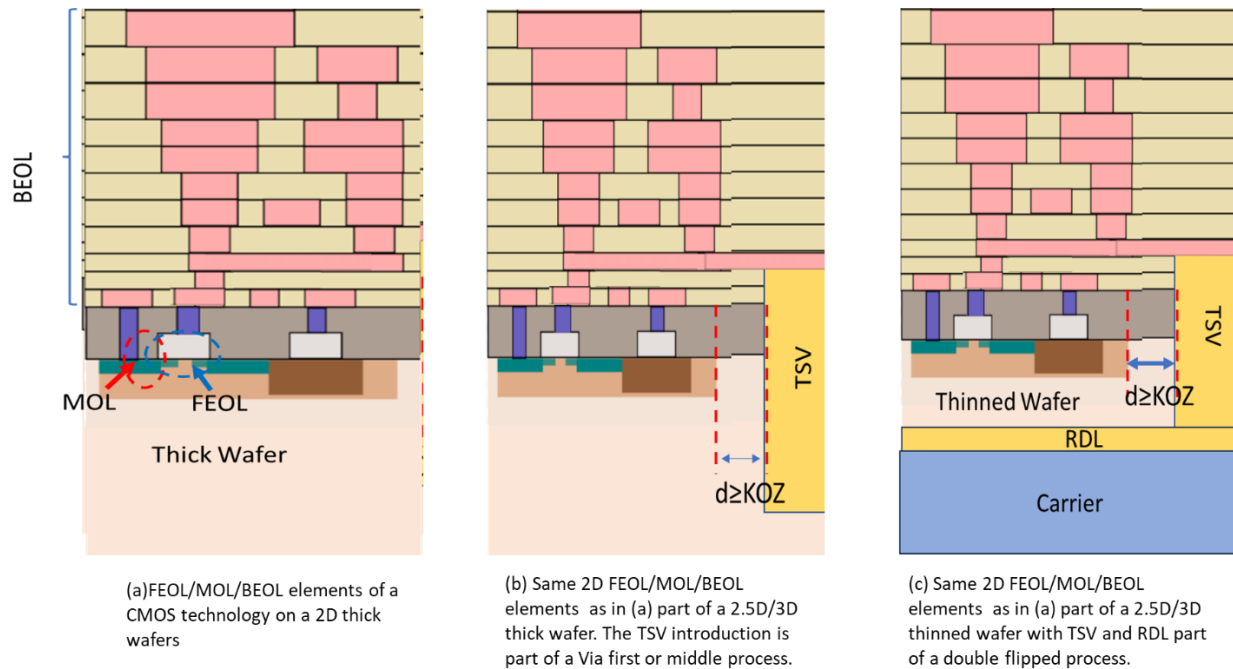
Figure 2 — Double Flipped 2.5D/3D Thinned Wafer Process

4.1 Stress and Test Vehicles (cont'd)

Figure 3 lists the three possible wafer configurations to be investigated as part of 2.5D/3D thinned wafer reliability evaluation with Cu-TSV, wafer thinning and RDL. These configurations are:

- 2D thick wafer,
- 2.5D/3D thick wafer with a TSV introduction by a TSV via first or middle process, and
- Double Flipped 2.5D/3D thinned wafer with Cu-TSV and RDL process.

In this case, the same FEOL/MOL/BEOL elements of a 2D IC processing are common between the three wafer configurations.



- 2D thick wafers.
- 2.5D/3D thick wafers.
- 2.5D/3D double flipped thinned wafers with TSV and RDL.

Figure 3 — List of Different Types of Wafer Configurations Used in this Publication with the Same 2D FEOL/MOL/BEOL Elements

d is the distance between the TSV and the FEOL/MOL/BEOL elements allowed by design outside the keep-out zone (KOZ). The wafer configuration in (b) and (c) with the 2D FEOL/MOL/BEOL structures placed far enough away from the TSV (typically $d \gg 10 \mu\text{m}$) describes what in this publication is defined as a reference device. In this case,

- A reference device in (b) is expected not to be exposed to TSV mechanical proximity effects.
- A reference device in (c) is expected not to be exposed to TSV mechanical proximity effects but still may be impacted by the RDL and wafer thinning process.

The reference devices distance from the TSV can be estimated from 2.5D/3D TCAD process and device simulation, but they should also be experimentally verified.

5 Impact of the Introduction of 2.5D/3D TSV/RDL/Wafer Thinning Processes to the Reliability of a 2D Qualified CMOS Technology

5.1 Objective

In this subclause, key guidelines are given to quantify the impact from the introduction of TSVs, wafer thinning and the Backside RDL part of a 2.5/2.5D/3D process to the reliability of the FEOL, MOL and BEOL elements on an already qualified 2D CMOS technology.

The evaluation of this impact amounts to running the same qualification stress/test activities completed in qualifying the reliability of the underlying 2D CMOS technology and quantify any possible difference in the reliability of the 2D base technology due to the introduction of the above 2.5D/3D elements.

The JEDEC publications JEP001-1A (BEOL/MOL) and JEP100-2A (FEOL) respectively give the key reliability guidelines to qualify a 2D foundry technology.

Two types of 2.5D/3D related effects need to be evaluated.

1) TSV mechanical proximity effects.

Mechanical proximity effects are due to the TSV mechanical (compressive and tensile) stress buildup as function of the distance (Typically $<<10\mu\text{m}$) between the 2D FEOL, MOL and BEOL structures and the TSV.

2) TSV/RDL and wafer thinning global effects.

Global effects are not associated with the mechanical stresses due to the TSV proximity but relate to the impact to the 2D qualified technology by the additional processing steps from both the TSV/RDL introduction and wafer thinning. In this publication we consider two types of global effects:

- a) Global effects associated with 2D devices that are not electrically connected to TSVs and/or the Redistribution Layer (RDL) part of 2.5D/3D processing. An example of these 2.5D/3D global effects is from the impact of the TSV and wafer thinning/RDL heat cycles during the 2.5D/3D wafers processing. These heat cycles are in addition to the 2D CMOS thermal budget and can worsen the reliability of the 2D technology elements. Reference 5.3.1 for details. Similar impact to the 2D BEOL levels “Via, Metals” formed before the TSV introduction can also be due to these global effects.
- b) Global effects associated with 2D devices electrically connected to TSVs and/or the Redistribution Layer (RDL) part of the wafer thinning. An example of these 2.5D/3D global effects is the impact to the 2D devices from possible Plasma Induced Damage during the 2.5D/3D processing. Reference 5.4 for details.

5.2 TSV Mechanical Proximity Effects

5.2.1 Recommended Structures

To evaluate the reliability impact to FEOL, MOL, BEOL devices from TSVs induced mechanical proximity effects, test structures need to be placed at a given distance from a TSV. These structures need to be designed similarly to the FEOL, MOL, BEOL test structures that were used for the underlying 2D reliability qualification.

This evaluation consists of the comparison of the device aging between devices that are at different distances and orientation from the TSV and 2D reference devices.

Figure 3 (c) gives a description of a DUT placed at a distance d from the TSV in the thinned wafers to be used for this evaluation.

An example for a given MOSFETs device, is given in Figure 4. In this case the Device Under Test (DUT) is placed at different distances and orientations from the center of a TSV and has the same layout of the 2D DUT used for the qualified underlying 2D technology. No electrical connection between the TSV and the DUT is allowed. Figure 4 gives a description for the case of the evaluation of FEOL intrinsic wear-out mechanism such as BTI, HC and Gate Dielectric TDDB.

As described in Figure 3, this comparison should be run as needed on:

- (a) 2D thick wafers.
- (b) 2.5D/3D thick wafers.
- (c) 2.5D/3D Double flipped thinned wafers.

Comparing the reliability of devices placed at different distances from the TSV, including the 2D reference devices, on 2.5D/3D Double flipped thinned wafers and on 2.5D/3D thick wafers will indicate if the intrinsic TSV proximity effects (2.5D/3D thick wafers) are impacted by the wafer thinning process (2.5D/3D Double flipped thinned wafers). A comparison between the reference devices on the 2.5D/3D Double flipped thinned wafers and 2D thick wafers will quantify the impact of the TSV, wafer thinning and RDL processing on the 2D devices due to the extra 2.5D/3D heat cycle. These 2D reference devices evaluations are a critical part of the 2.5D/3D “global effects” that do not relate to TSV mechanical proximity.

5.2.1 Recommended Structures (cont'd)

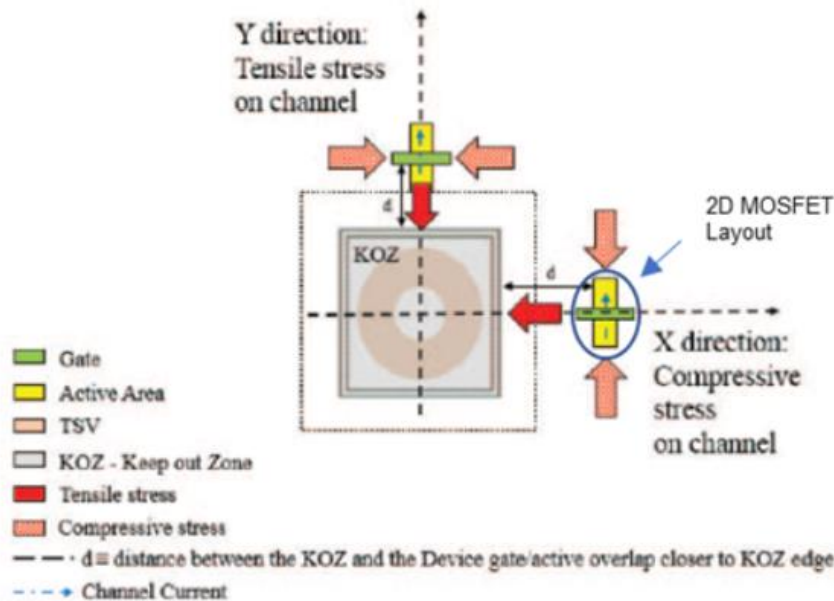


Figure 4 — Example of 2.5D/3D Design to be Used to Investigate TSV Induced Mechanical Proximity Effects on MOSFET Device Reliability

The basic MOSFET device layout is the same as the one used for the 2D qualification. No electrical connection between the TSV and the device under test is allowed.

5.2.2 Standard Guidelines

- 1) Verification of 2D Reliability dependence on device placement for a given distance from TSVs.
- 2) The structures to be used for TSV mechanical stress evaluations (compressive/tensile stress) need to take into account the stress profile in an isolated and nested TSV environment.
- 3) Reference devices are Device Under Tests placed far away from the TSVs ($d > 10 \mu\text{m}$) so that the reference devices are not impacted by proximity effects. These reference devices also need to be included as part of the stress/test to estimate global effects.
- 4) Selection of these structures to be used for 2.5D/3D FEOL/BEOL/MOL Reliability evaluation should be consistent with the ones used for the 2D POR qualification.

5.3 TSV/RDL Global Mechanical Effects

5.3.1 Global Effect Associated with 2D Devices not Electrically Connected to TSV and/or RDL

An example of these global effects is given in Figure 5. In this case the potential impact to Channel Hot Carrier (CHC) from these types of global effects on a reference thick oxide n-MOSFET is given. Notice that the increase in CHC of 2.5D/3D thick wafers with respect to 2D thick wafers indicates the impact of the TSV heat cycles to CHC as part of the TSV introduction. While the increase in CHC between the 2.5D/3D thick and 2.5D/3D thinned wafers with RDL processing indicated further CHC enhancement should be investigated to offset the impact due to the wafer thinning and RDL processing heat cycles.

5.3.1 Global Effect Associated with 2D Devices not Electrically Connected to TSV and/or RDL (cont'd)

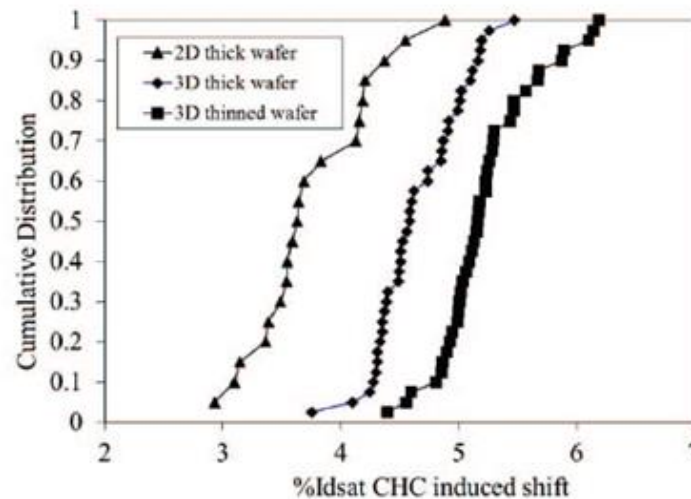


Figure 5 — Impact to the CHC on an nMOSFET Reference Device after the TSV Introduction, Wafer Thinning and RDL Processing

Larger CHC degradation is measured in 3D thinned wafers compared to 3D and 2D thick wafers.

The comparison of the deltas of the intrinsic wear-out mechanisms under investigation between the three different wafers options can be used to define the TSV Keep Out Zone (KOZ) as the area outside which the 2.5D/3D FEOL/MOL/BEOL reliability of a given device will be similar or acceptable within the 2D reliability End of Life (EOL) targets.

5.3.2 Global Effect Associated with 2D Devices Electrically Connected to TSV and/or RDL

An example of global effects associated with 2D devices electrically connected to TSV and/or RDL is discussed in 5.4.

5.4 TSV/RDL Plasma Induced Charging Damage (PID)

The introduction of the TSVs and Backside RDL on 2D thinned wafers can be a source of Plasma Induced Damage (PID). This is in addition to what can be experienced by a 2D device during the BEOL 2D processing. This is an example of global effects with the 2D DUT electrically connected to both the TSV and/or Backside RDL.

The PID impact due to plasma etching and the plasma deposition process during the TSV/RDL steps, as well as wafer thinning strongly depends on the adopted TSV process.

In particular:

Via First and Via Middle TSV process

- The 2D devices are not electrically connected to TSVs during TSV formation.
- Possible PID charging can only be due to the wafer thinning and the Backside RDL metal process.

5.4 TSV/RDL Plasma Induced Charging Damage (PID) (cont'd)

Via last TSV process

- Since the TSV introduction is done after the 2D wafer is thinned and before the RDL deposition, possible charging may be due to both TSV formation after wafer thinning and the Backside RDL metal process.

Figure 6 is a graphical description of the expected 2.5D/3D PID sensitivities to the adopted TSV process.

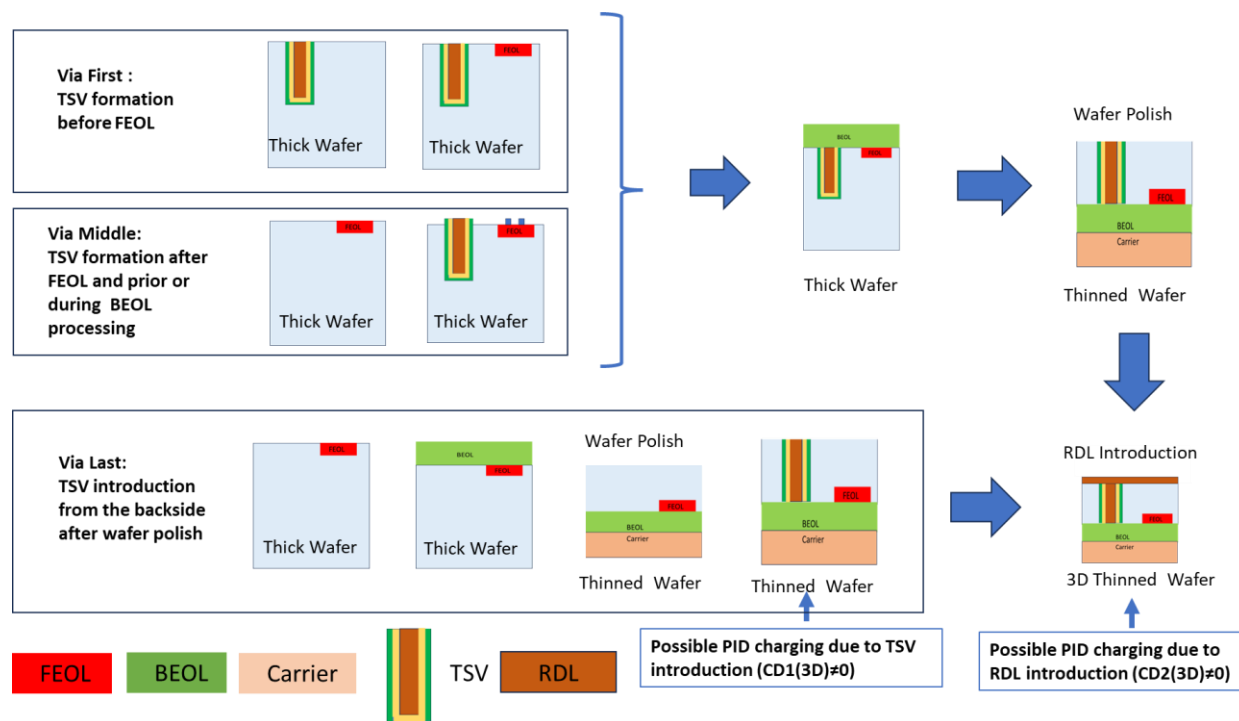


Figure 6 — 2.5D/3D PID Dependence on the TSV/RDL Processes

5.4.1 PID Antenna Rules

Key output of the 2.5D/3D PID evaluation is the estimation of the PID antenna rule to be used as part of the 2.5D/3D circuit design.

A key assumption in defining the 2.5D/3D antenna rules is that the same antenna rules formulation as defined for the 2D thick wafers of the 2D underlying technology needs to be satisfied in the 2.5D/3D environment.

This 2.5D/3D antenna rule definition includes the contribution of the TSV and/or Backside RDL metal plasma etching by an effective TSV and RDL area contribution. It is assumed that the wafer thinning process does not contribute to the 2.5D/3D PID.

5.4.1 PID Antenna Rules (cont'd)

As an example, equation 2 gives a possible definition of 3D gate metal area antenna rule with a formulation equivalent to the corresponding 2D counterpart (equation 1). If this gate antenna rule is used, then for a given active gate area ($Gate_{Area}$) connected to a total TSV area (TSV_{Area}) and Backside RDL area (RDL_{Area}) as well as a given BEOL Metal area ($Metal_{Area}$), the Diode/Junction area ($Junction_{Area}$) needs to guarantee that the Antenna Ratio (AR) for the 2D antenna rule ($AR_{(2D)}$) is satisfied. The $Gate_{Area}$ is the cumulative area of all active gates connected to the circuit node.”

In other words, the 3D design needs to satisfy the 2D design manual antenna rules.

$$\frac{Metal_{Area}}{Gate_{Area} + C3(2D) \times Junction_{Area}^{(2D)}} \leq AR_{(2D)} \quad (1)$$

$$\frac{Metal_{Area} + (C1(3D) \times TSV_{Area} + C2(3D) \times RDL_{Area})}{Gate_{Area} + C3(3D) \times Junction_{Area}^{(3D)}} \leq AR_{(2D)} \quad (2)$$

Where:

- $AR_{(2D)}$ is the Antenna Ratio (AR) allowed by the 2D Design Manual.
- The impact factors $C1(3D)$ and $C2(3D)$ weigh the PID extra contribution with respect to the PID effect from the 2D processing.
- The Junction area includes both the area of any diffusion (Source/Drain) connected to the gate and possible diode area used for PID protection.
- The areas of metal, TSV, RDL and gate, junction are defined in μm^2 .

The PID impact due to plasma etching (or plasma enhanced layer deposition) during the TSV processing is addressed by the impact factor $C1(3D)$ in equation 2 while the impact due to plasma etching (or plasma enhanced layer deposition) during the RDL processing steps are addressed by the impact factor $C2(3D)$ in equation 2. A possible change in the diode/junction efficiency due to the 2.5D/3D processes respect to 2D is represented by the parameter $C3(3D)$.

The constants $C1(3D)$, $C2(3D)$ and $C3(3D)$ must be experimentally determined during the 3D process qualification from fully processed (including complete RDL and TSV) thinned 2.5D/3D wafers.

The constant $C1(3D)$ is very much dependent on the TSV process option.

Please note that in a TSV via-first or via-middle process the impact factor $C1(3D) = 0$ because of no contribution from TSV plasma processing on the transistors (as shown in Figure 6). However, In the TSV via last process $C1(3D) > 0$.

Notice that $C2(3D) > 0$ for all the 3 different TSV process options.

The above 3D formulation (equation 2) is only an example for a 3D Gate antenna rule. Other 3D antenna rules formulations are possible. In any case, the 2.5D/3D processes must satisfy any qualified Design Manual 2D antenna rules.

5.4.1 PID Antenna Rules (cont'd)

This PID evaluation only covers any antenna charging coming from the wafer thinning with TSV/RDL metal charging, and plasma charging and deposition. It does not take into account any charging coming from other 2.5D/3D integration elements such as wafer stacking, 2.5D/3D packaging, etc.

5.4.2 Structures to be used for the 2.5D/3D PID Evaluation

Two types of structures are recommended for an adequate 2.5D/3D PID evaluation. As an example, we provide the details of a TSV Via last process in Figure 7 with the DUT being an nMOSFET device.

In this case the following structures should be used:

- 1) 2.5D/3D PID structure in a double flipped wafer with TSV, RDL, Mx area and diode area to satisfy equation 2. In this case the TSV/RDL metal is connected to the nMOSFET gate by BEOL wiring up to Metal 3 (M3) formed before the TVS introduction. The DUT is placed far away from the KOZ to minimize possible TSV mechanical proximity effects. The gate is protected by diode.
- 2) Same structures as in (a) but without diode protection.

In Figure 7, structures (c) and (d) describe the corresponding structures described in (a) and (b) with the DUT gate not connected to the TSV. Both options with (c) and without (d) diode protection are given. This implies, for example, that the TSV/RDL is not charging. $C1(3D) = C2(3D) = 0$ in equation 2.

This is an example of reference 2D structures in thinned double flipped wafers to be used as a baseline to investigate the possible PID enhancement due to the TSV and RDL introduction in structures (a) and (b) described in Figure 7.

All structures (a) through (d) should be available on the same wafer.

5.4.2 Structures to be used for the 2.5D/3D PID Evaluation (cont'd)

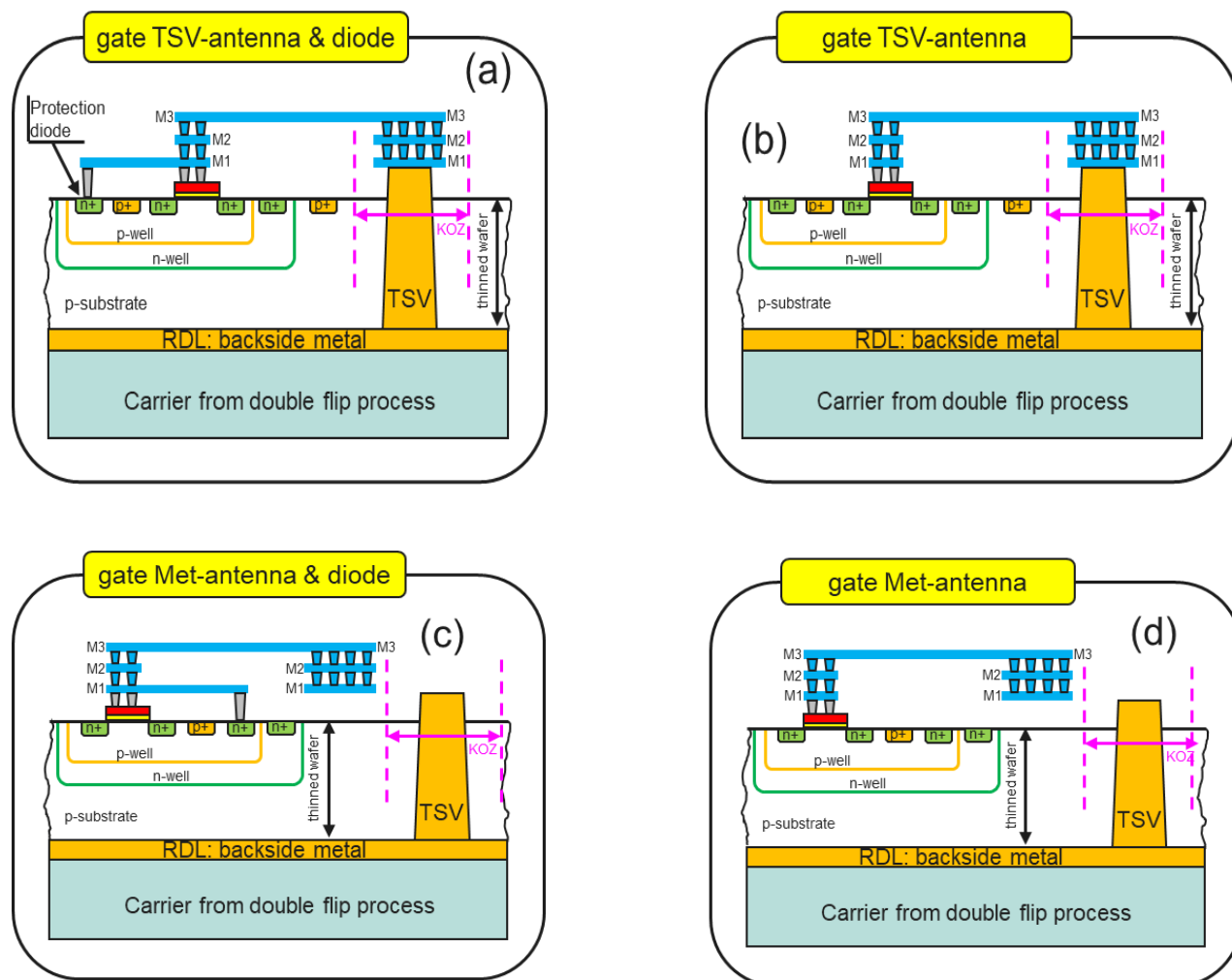


Figure 7 — Two 2.5D/3D Structures Recommended for 2.5D/3D PID Evaluation

As an example, a cross-section of an nMOSFET transistor with TSV via last and RDL-antenna (a) with and without protection diode (b) are given. In Figure 7, structures (c) and (d) describe the corresponding structures described in (a) and (b) with the DUT gate not connected to the TSV. These two structures are an example of a reference structures that could be used to evaluate the PID 2D baseline in a thinned wafer with a double flipped process.

5.4.3 Key PID Analysis

Comparison of as processed last metal device parameters (V_{th} , I_{dsat} , Gate leakage, etc.) and FEOL Reliability (TDDDB, BTI, HC, etc.) between structure (a) and structure (b) in Figure 7 to estimate the PID extra contribution to the 2.5D/3D process.

The acceptable deltas between structure (a) through (d) are based upon agreement between supplier and customer.

5.5 Stress/Test Reliability Guidelines

To qualify a given reliability intrinsic wear-out mechanism against the 2.5D/3D TSV mechanical proximity and global effects (Ex. TSV/Thinned Wafers/RDL PID effects) it is recommended to run the same Reliability tests and stresses sequence used to qualify this wear-out mechanism in the underlying 2D CMOS technology including PID. In this case all the 2D intrinsic wear-out mechanisms associated with the 2D baseline reliability evaluation need to be included as part of the 2.5D/3D qualification. The same basic structures/devices layout used in the 2D technology qualification need to be used in the 2.5D/3D structures to be used for the 2.5D/3D qualification as well.

5.6 Hardware Requirements

To qualify a given reliability intrinsic wear-out mechanism against the 2.5D/3D TSV mechanical proximity and global effects the same hardware requirements (# wafers/lot, # lots) needed for the qualification of this wear-out mechanism on the underlying qualified 2D CMOS technology is recommended (e.g., same hardware requirements for the PID evaluation in the 2D and 2.5/3D technology qualification).

5.7 Parameters to Monitor.

The same FEOL device reliability parameters evaluated as part of the 2D Reliability evaluation should be used when evaluating each 2.5D/3D process impacting 2D PID.

5.8 Fail Criteria

The same FEOL fail criteria defined for the 2D Reliability evaluation for each 2.5D/3D process impacting 2D Reliability.

5.9 Deliverables

Report on stress, test, and data analysis.

Same characterization done on 2.5D/3D as was done on 2D.

Example: If the PID key parameter is the MOS gate dielectric leakage, then the gate leakage for the 2.5D/3D must meet the same specification as that based upon 2D learning. Give details on the antenna structures used for the 2.5D/3D PID evaluation and difference with the 2D PID structures.

6 TSV Electromigration (EM) Guidelines on Wafers with TSV – Wafer Thinning

6.1 Reliability Evaluation

The main focus of this publication is to give guidelines on the evaluation of the key 2.5D/3D process contributors to the intrinsic Electromigration from both the Cu TSV and the Cu TSV interface levels as follows:

- 1) Cu TSV
- 2) RDL/TSV interface
- 3) Mx/TSV interface

Figure 8, Figure 9, and Figure 10 give guidelines of the DUT designs to evaluate 1), 2) and 3), respectively.

6.2 Stress Recommendations

A Module Level Stress (MLS) is recommended as a sanity check test on modules from 2.5D/3D double flipped thinned wafers at constant current stress (I_{stress}) for a given stress temperature (T_{stress}) and stress time (t_{stress}). The sanity check test is performed with the expectation that no failures will occur within the defined test time (t_{stress}).

The following guidelines are given for the MLS stress:

- a) Module Level Stress (MLS) = Stress of the selected 2.5D/3D TSV EM DUTs that are part of a double flipped thinned wafer with pads wire bonded to a proxy package.
- b) For the adopted TSV DUT structure, the Backside RDL and/or Mx metals part of the testing pads need to be designed such that, at the selected I_{stress} , no fails are associated with the pads during the t_{stress} at the T_{stress} . See the recommended structures below for an example of how to engineer each of the pad elements including Mx and Backside RDL accordingly.
- c) $T_{stress} < T_{max}$, where T_{max} is the maximum temperature that will prevent any damaging (warping) during the TSV EM module level stress within the selected t_{stress} . Depending on the TSV thinning process, a T_{stress} close the typical T_{stress} for EM Copper BEOL reliability stressing (280 °C–300 °C) could be selected.
- d) For a given I_{stress} and T_{stress} , the stress time (t_{stress}) should be selected to ensure that achieving 0 fails after t_{stress} implies that the EOL failure rate due to the intrinsic EM of the Cu TSV, the TSV/Mx and the TSV/RDL interface levels is much smaller than the pre-defined target failure rate assumed for the product. This t_{stress} estimation could assume that Cu TSV intrinsic EM modeling is similar to the Cu EM BEOL (Typical $\Delta H \approx 0.7$ eV–1.0 eV, $n \approx 1$ –2 (the current density exponent in Black's law)). It is important to note that these EM model parameters need to be appropriate for the metallurgical stack being tested.

6.3 Recommended Structures

Below are some general guidelines for designing DUT test structures with Kelvin contacts to be used in evaluating the Cu TSV, the RDL/TSV and the Mx/TSV interface contributors to EM. The DUT structures given in Figure 8, Figure 9, and Figure 10 should be designed to reproduce the TSV/RDL/Mx configurations used in the product under evaluation.

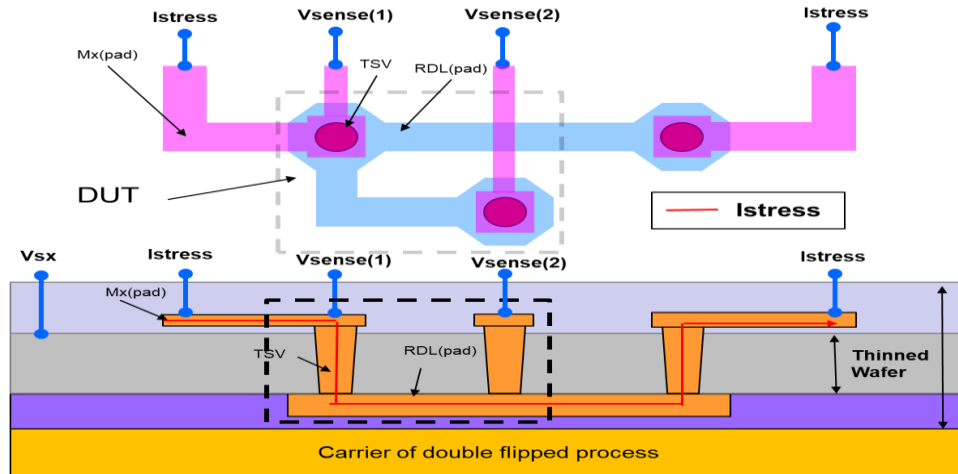


Figure 8 — Example of Recommended Structure for Cu-TSV EM Evaluation

- DUT defined by one TSV.
- The Backside RDL (pad) and any Mx(pad) metals connecting to the DUT under test needs to be designed to handle large Current/Current Density, such that there are no RDL and/or Mx failures occur during the I_{stress} for a given t_{stress} at the temperature T_{stress} .
- The number of DUTs to be stressed needs to satisfy the hardware requirements as discussed in the Hardware coverage clause below.

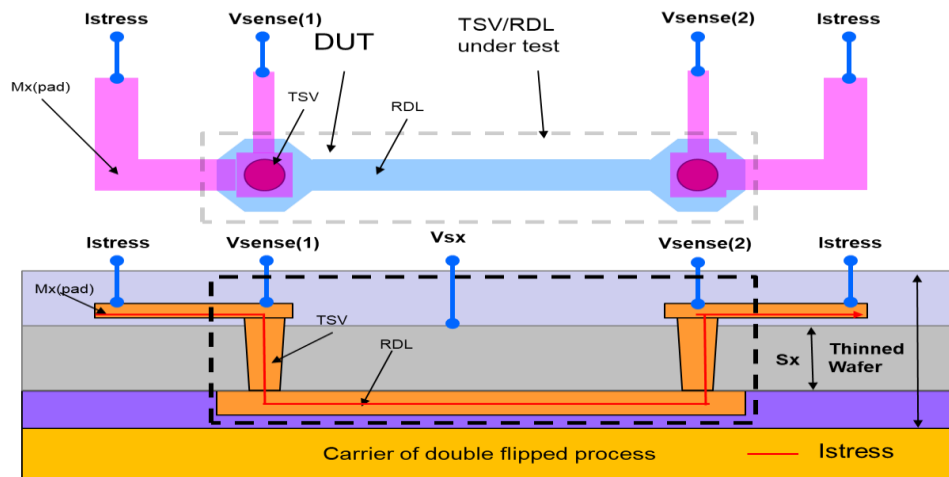


Figure 9 — Example of Structure to be Used to Evaluate the TSV/RDL EM

- DUT defined by TSV + RDL + TSV in series.

6.3 Recommended Structures (cont'd)

- Mx(pad) metals connecting to the TSVs under test need to be designed to handle large Current/Current Density, such that there are no Mx failures occur during the I_{stress} for a given t_{stress} at the temperature T_{stress} .
- RDL layer part of DUT to be designed with width and length ($L_{RDL} > \text{Blech Length}$) combinations allowed by 2.5D/3D Design Manual.
- The number of DUTs to be stressed needs to satisfy the hardware requirements as discussed in the Hardware coverage clause below.

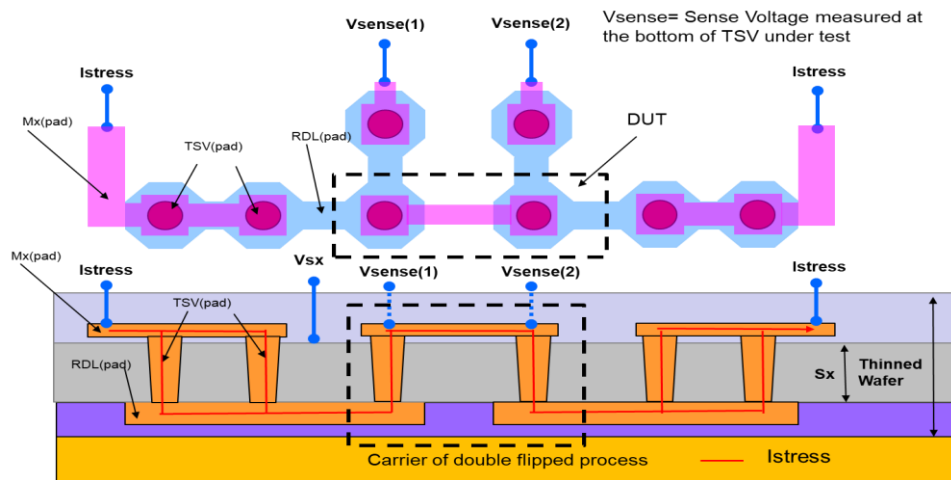


Figure 10 — Example of Structure to be Used to Evaluate the TSV/Mx EM

- DUT defined by TSV + Mx levels + TSV on series.
- Mx metals that are part of the DUT need to be designed with combinations of Mx width and length ($L_{Mx} > \text{Blech Length}$) allowed by the 2.5D/3D design manual.
- Possible Mx extrusions monitors could be included as part of the DUT.
- The Backside RDL (pad), the Mx(pad) metals and any number of TSV (pads) connecting to the DUT being tested needs to be designed to handle large current/current density, such that no RDL (pad), Mx(pad) and TSV (pad) outside of the DUT being tested fails during the I_{stress} for a given t_{stress} at the temperature T_{stress} .
- The number of DUTs to be stressed needs to satisfy the hardware requirements, as discussed in the Hardware coverage clause below.

6.4 Hardware Coverage

At the selected I_{stress} , t_{stress} , T_{stress} bias configurations the total number of DUTs to be stressed needs to assure, within a defined confidence level, that 0 fails after t_{stress} implies that the EOL failure rate due to intrinsic EM TSV is much smaller than the pre-defined target failure rate associated with the DUT structures under test. As a guideline for EM, JEP001 proposes a minimum of 20 modules/wafer over 3 wafers/lot, for 3 wafer lots. The number of modules/wafers should depend on the number of TSVs selected for a given DUT to be stressed.

6.5 Parameter to Monitor

Both %Resistance changes and leakage due to extrusions increase as measured from the recommended 2.5D/3D TSV structures (See Figure 8, Figure 9, and Figure 10).

6.6 Fail Criteria

The failure criteria will be either a predetermined increase in resistance, an open, or an increase in the leakage current associated with the TSV, RDL, and Mx structures to which the 2.5D/3D EM stress is applied.

Where: $R = ((V_{sense(2)} - V_{sense(1)})/I_{stress})$ and $I_{leakage} = I_{sx}$

Refer to Figure 8, Figure 9, and Figure 10 for definition of $V_{sense(2)}$ and $V_{sense(1)}$.

If EM fails are observed anywhere in TSV/RDL/Mx test structure, then process optimization is needed to pass the failure criteria. Failure Analysis should be done on any observed failures to verify the root-cause and failure location in the cross-section shown in Figure 8 through Figure 10.

6.7 Deliverable

Report on stress, test, and data analysis using the same characterization done on 2.5D/3D elements.

Example: If the key parameter is resistance increase, then this needs to be guaranteed that it is in spec for 2.5D/3D process assumptions.

The following could be included in the TSV electromigration results:

Materials and Geometries

- TSV Composition, Height & Diameter (Top & Bottom)
- RDL Composition, Height and Width
- Mx Composition, Height and Width

Failure Criteria

- # of Fails, % Resistance Change, $I_{leakage}$.

NOTE Test Assumes 0 fails.

Test Criteria

- Sample Size
- Oven Temperature (T_{stress})
- Stress Current (I_{stress})
- Length of Test (t_{stress})
- Initial Resistance, $I_{leakage}$
- Temperature rise of DUT due to Joule Heating (You need to describe this in the stress paragraph)

7 Dielectric/Metallic Liner/RDL & TSV Integrity

7.1 Reliability Evaluation

Both the intrinsic and extrinsic reliability of the 2.5D/3D TSV Dielectric/Metallic liner needs to be evaluated. A TSV intrinsic integrity evaluation as related to TDDB needs to be implemented as part of the 2.5D/3D TSV Dielectric/Metallic liner qualification. An appropriate Constant Voltage Stress (CVS) stress test matrix needs to be done to make sure that the intrinsic reliability meets the EOL criteria for a given application space. While Intrinsic TDDB is not expected to impact the reliability of the product, at a minimum check, it is recommended to use multiple voltage ramp stress (VRS) to detect any TSV process induced intrinsic and extrinsic fails.

Figure 11 describes the TSV array layout of the recommended structure to be used for both the TDDB and VRS. Failure Analysis should be done on any observed failures to verify the root-cause and failure location in the cross-section shown in Figure 11 through Figure 13.

7.2 TSV Structures to be Evaluated

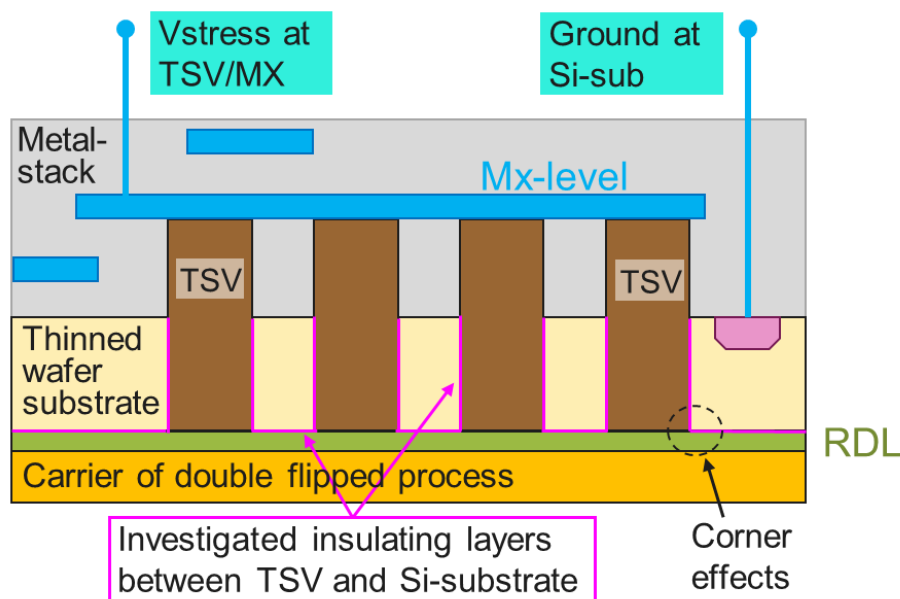


Figure 11 — Example of TSVs Array Layout to be Used to Evaluate the TSV Dielectric/Metallic Liner and TSV/RDL Dielectric Integrity in a 2.5D/3D Thinned Double Flipped Wafer

- Number of TSVs in parallel selected to satisfy a given area requirement.as discussed in the Hardware coverage clause.
- Grounded Substrate bias is required.
- This test structure is valid for all Via TSV processes.

Arrays of TSVs in 2.5D/3D thick and/or 2.5D/3D thinned wafers are suggested to differentiate between the contributions from the existing different dielectric isolations. It is recommended to implement arrays with different numbers of TSV which represent different areas of dielectric isolation for area scaling of the breakdown voltage distributions. A probing pad with a substrate connection is needed (refer to Figure 11 through Figure 13).

7.2 TSV Structures to be Evaluated (cont'd)

Figure 12 describes a complementary test structure layout to assist in determining if back grinding is contributing to any observed TDDB or VRS fails detected using the structure in Figure 11.

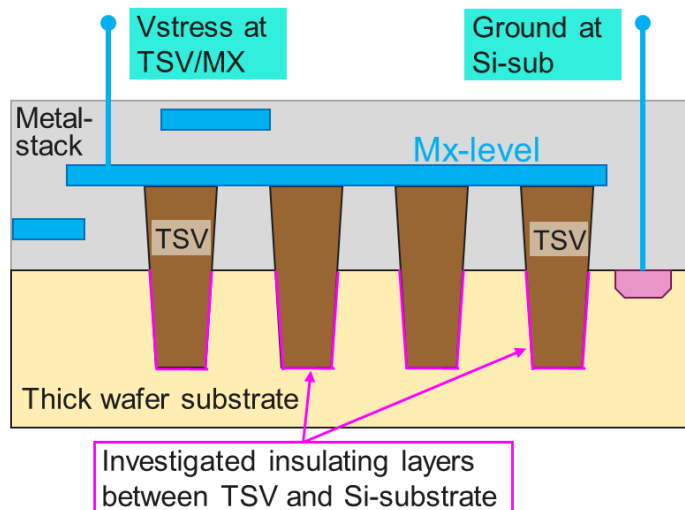


Figure 12 — Example of TSVs Array Layout to be Used to Evaluate the TSV Dielectric/ Integrity in a 2.5D/3D Thick Wafer

- Number of TSVs in parallel selected to satisfy a given area requirement, as discussed in the Hardware coverage clause.
- Grounded Substrate bias is required.
- This test structure is valid only for Via first and middle TSV Via processes.

Figure 13 describes a complimentary test structure layouts to assist in determining if the RDL process is contributing to any observed TDDB or VRS fails detected using the structure in Figure 11.

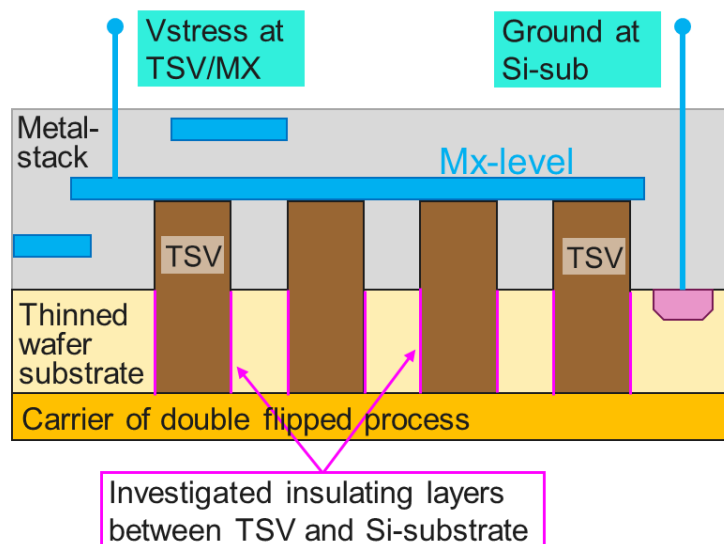


Figure 13 — Example of TSVs Array Layout to be Used to Evaluate Only the Dielectric Integrity Between TSV and Si Substrate with no RDL Contribution in a 2.5D/3D Thinned Double Flipped Wafer

7.2 TSV Structures to be Evaluated (cont'd)

- Number of TSVs in parallel selected to satisfy a given area requirement, as discussed in the Hardware coverage clause.
- Substrate bias required.
- This test structure is valid for all Via TSV processes.

7.3 Stress

At a minimum, a CVS stress/test matrix for TDDDB and VRS at a selected stress temperature is recommended. This stress temperature should be derived from the required temperature profile of the technology's mission profile. Typically, $T = 125^\circ\text{C}$ is a foundry standard, but the maximum temperature at the technology application conditions should be checked as was done for the 2D qualification baseline.

Both accumulation (Cu confinement mode with $V_{stress} < 0$ inside TSV, $V_{ground} = 0\text{ V}$) and inversion mode (Cu drive in mode with $V_{stress} > 0$ inside TSV, $V_{ground} = 0\text{V}$) should be evaluated.

V_{max} for VRS stress is selected by the customer-supplier agreements to screen to a given extrinsic defect density on a defined total TSV area, TSV leakage, sample size and VRS procedure.

7.4 Hardware Coverage

2.5D/3D thick (recommended) + thinned wafers with Carrier of double flipped process (required). Same sample size typically required for 2D gate oxide VRS evaluation is recommended.

7.5 Parameters to Monitor

Cu-TSV, TSV/Mx, TSV/RDL leakage and V_{max} .

7.6 Deliverable

V_{max} to a given defined leakage increase ($I_{lkg-max}$)

Report on VRS and test conditions:

- VRS waveform
- Cu-TSV, TSV/Mx, TSV/RDL leakage measured at use conditions during VRS.
- Leakage increase ($I_{lkg-max}$) associated with V_{max} (VRS voltage at $I_{lkg-max}$)
- Sample Size
- Stress Temperature (T_{stress})
- Initial $I_{leakage}$

Materials and geometries:

- TSV Composition, Height & Diameter (Top & Bottom)
- RDL Composition, Height and Width
- Mx Composition, Height and Width

8 2D WLR Elements – BEOL Reliability in a 2.5D/3D Thinned Wafer – Stress Migration and Thermal Cycle

8.1 SM and TC Reliability Evaluation

To evaluate the impact of Stress Migration (SM) and Thermal Cycle (TC) to the 2D BEOL reliability of an IC fabrication due to the introduction of the 2.5D/3D processes part of thinned wafers (Cu-TSVs, wafer thinning and the RDL process).

Given that SM and TC stressing is typically required as part of a 2D BEOL reliability technology/process qualification, this activity completes the 2.5D/3D requirements to qualify the 2D BEOL Reliability as part of the 2.5D/3D processes described in this document.

This clause is an addition to clause 5 to include guidelines for the SM and TC as part of the 2D BEOL reliability evaluation with the 2.5D/3D introduction.

Testing is done on 2.5D/3D thinned wafers with a double flipped process using either Wafer (WLR) or Module Level Reliability Stress (MLS). MLS testing was discussed in clause 6.

It is assumed that the 2.5D/3D BEOL to be evaluated is similar to the BEOL qualified as part of the 2D technology baseline. In this case the same SM and TC testing procedures adopted to qualify the 2D BEOL will be used to qualify the 2.5D/3D BEOL when possible.

If the initial 2D BEOL technology qualification didn't require BEOL SM and/or TC stress, then 2D thick wafers can be used as a control when evaluating any impact to the 2D BEOL technology due to the addition of 2.5/3D elements.

Key focus needs to be paid on making sure that the locations of 2.5D/3D BEOL structures relative to the TSVs are consistent with the 2.5/3D Design Manual rules (Keep out zone, etc.). As a guideline, the recommended structures and hardware requirements described in clause 5 for the TSV mechanical proximity evaluation are recommended. See Figure 3 as a reference.

The areas of concern include, but are not necessarily limited to, TSV Cu Pumping, BEOL Stressed Induced Voiding (SIV) and delamination after SM and TC stress.

8.2 Hardware Coverage

For both the SM and TC reliability evaluation, multiple double flipped thinned wafers are needed. Multiple 2D thick wafers can be used as a control as also testing 2D BEOL structures is recommended. The sample size should be the same as the one needed for the 2D BEOL SM and TC qualification. Typical hardware requirement of 3 lots, 3 wafers/lot, 20 to 40 sites/wafer is recommended.

8.3 Structures to be Evaluated

The test structures to be used for the 2.5D/3D BEOL SM and TC stressing as described in clause 5 are given as guidelines, The 2.5D/3D BEOL structures should have similar design as for the 2D BEOL ones. Details on the designs of 2D BEOL test structures are not given in this document. Figure 4 gives an example of 2D and 2.5D/3D structures to be designed for a FEOL reliability evaluation. A similar approach should be used for a BEOL reliability evaluation including SM and TC.

8.4 Parameters to Monitor

The same BEOL parameters evaluated as part of the 2D Reliability evaluation should be used when evaluating each 2.5D/3D process impacting 2D BEOL Reliability.

8.5 Deliverable

Report on stress, test, and data analysis using the same characterization done on 2.5D/3D elements as was done on 2D elements. Ex: if the key param is delta resistance, then it needs to be guaranteed that it is in spec for 2.5D/3D process based upon 2D learning.

8.6 Stress Migration (SM) Details

For both the 2D BEOL and 2.5D/3D, it is recommended that the BEOL test structures be exposed to Stress Migration at a given stress temperature (T_{stress}) for 1000 hours-2000 hours (t_{stress}). The same SM temperatures need to be used on the 2.5D/3D wafers and the 2D process qualification before TSV/RDL processing. Due to concerns about damage due to warpage of the thinned wafer/carrier, a T_{stress} within the range of 175 °C-275 °C is recommended. If a different range of T_{stress} is used for the 2.5D/3D wafers, then similar data at this range of T_{stress} for the 2D processed wafer without the TSV/RDL processing is also needed. Data to support the T_{stress} selection to be provided as part of the report.

For additional information and foundry guideline on SM, the reader can refer to JEDEC JEP001-1A, as well as to JESD214.

8.7 Thermal Cycle (TC) Details

For both the 2D BEOL and 2.5D/3D, it is recommended that the BEOL test structures to be exposed to the same TC stress and test methodology adopted for the 2D technology qualification. Typically, a TC stress with a T_{stress} cycle of = -65 °C to +150 °C for 1000 cycles is adopted.

For additional information and foundry guidelines on TC, the reader can refer to JEDEC JEP001-1A, as well as JSD47 and JESD22A-104.

9 2.5D/3D WLR Elements – TSV Reliability and Latency Impact to FEOL and MOL - High Temperature Storage/SM and TC

9.1 Reliability Evaluation

This clause gives guidelines on extra SM and TC activities required in a 2.5D/3D technology/process qualification with thinned wafers elements (Cu-TSVs, wafer thinning and the RDL process) in addition to what described for BEOL in clause 8.

These extra SM and TC activities consist of:

- SM and TC effect on Cu TSV, TSV/RDL & TSV/Mx interface integrity.
- SM and TC possible latency impact to the reliability of FEOL/MOL part of the 2.5D/3D IC design.

9.1 Reliability Evaluation (cont'd)

In this context the SM activity can be equivalent to what is typically done for Wafer Level High Temperature Storage (HTS) stress. The SM guidelines recommended in this publication apply for HTS as well.

It is assumed that the same SM and TC testing procedures adopted to qualify the 2D BEOL will be used to qualify the 2.5D/3D reliability items.

Testing is done on 2.5D/3D thinned wafers with a double flipped process using either Wafer (WLR) or Module Level Reliability Stress (MLS). MLS testing was discussed in clause 6.

The evaluation of the impact from HTS/SM and TC to the Cu TSV, TSV/RDL and TSV/Mx interface integrity is unique of a 2.5D/3D process.

The Cu TSV, TSV/RDL and TSV/Mx structures to be evaluated as part of the 2.5D/3D HTS/SM and TC stress should be similar to what is recommended in clause 7. Thick wafers with Cu TSV need to be used as a control when evaluating any impact on the TSV/RDL and TSV/Mx interface. Guidelines on 2.5D/3D structures to use, Parameters to monitor and hardware requirements are given in clause 7 as well.

The evaluation of any impact from both HTS/SM and TC to the 2D FEOL and MOL technology after the 2.5D/3D process introduction amounts to running the same stress and test procedures adopted in the original qualification for the underlying 2D FEOL and MOL technology post HTS/SM and TC as described in clause 5.

The 2D FEOL and MOL structures to be evaluated as part of the 2.5D/3D HTS/SM and TC stress should be similar to the ones used as part of the original 2D qualification and designed on thinned wafers with the TSV and RDL introduction. Since typically the 2D FEOL/MOL thick wafer qualification does not require SM and TC, 2D Thick wafers need to be used as a control when evaluating any impact on the 2D FEOL and MOL technology due to the addition of 2.5D/3D elements. Guidelines on the structures to use, hardware requirements and parameters to monitor are given in clause 5.

9.2 Hardware Coverage

Multiple thinned wafers with carrier from a double flipped process are needed. Multiple 2D thick wafers can be used as a control, if needed. It is recommended that the sample size to be the same as the one needed for the 2D qualification. Typical hardware requirement of 3 lots, 3 wafers/lot, 20 to 40 sites/wafer is recommended. Further details can be found as follows:

- Cu TSV, TSV/RDL, TSV/Mx integrity -Hardware requirements in clause 7.
- FEOL/MOL latency effects – Hardware requirements in clause 5.

9.3 TSV Structures to be Evaluated

- Cu TSV, TSV/RDL, TSV/Mx integrity-Array of TSVs in 2.5D/3D thick and/or 2.5D/3D thinned wafers (clause 7).
- FEOL/MOL latency effects - Same Structures used for Mechanical TSV proximity (clause 5)

9.4 Parameters to Monitor (TSV integrity)

- Cu TSV, TSV/RDL, TSV/Mx integrity - TSV leakage, V_{max} (clause 7) before and after SM and TC.
- FEOL/MOL latency effects – Key FEOL/MOL RE parameters shifts as described in clause 5 before and after HTS and TC.

9.5 Deliverable

Report on stress, test, data analysis as well as model assumptions using the same characterization done on 2.5D/3D elements as was done on 2D elements where it applies.

- For MOL/FEOL latency effects from HTS/SM and TC the same deliverable as indicated in clause 5 are required.
- For Cu TSV, TSV/RDL, TSV/Mx integrity from HTS/SM and TC the same deliverable as indicated in clause 7 are required.

9.6 HTS/SM Details

Consistent to what is described in clause 8, for both the 2D FEOL and MOL latency effects and the CU/TSV, TSV/RDL and TSV/Mx interface integrity due to HTS/SM stressing, it is expected that thinned wafers be exposed to an elevated temperature (T_{stress}) for 1000 hours-2000 hours (t_{stress}). Attention must be paid so that $T_{stress} \leq T_{max}$, where T_{max} is the maximum temperature that will prevent any damaging (warping) of the thinned wafer/carrier during the TSV HTS test within the selected t_{stress} . Thus, due to these concerns about damage due to warpage of the thinned wafer/carrier, a T_{stress} within the range of 175 °C-275 °C is recommended. If a different range of T_{stress} is used for the 2.5D/3D wafers, then similar data at this range of T_{stress} for the 2D processed wafer without the TSV/RDL processing is also needed. Data need to be provided to support the T_{stress} selection as part of the report.

For additional information and foundry guideline on HTS, the reader can refer to JESD22-A103.

9.7 Thermal Cycle (TC) Details

Consistent to what is described in clause 8, for both the 2D FEOL and MOL latency effects and the CU/TSV, TSV/RDL and TSV/Mx interface integrity due to TC stressing, it is recommended that the BEOL test structures be exposed to the same TC stress and test methodology adopted for the 2D technology qualification. Typically, a TC stress with a T_{stress} cycle of -65 °C to +150 °C for 1000 cycles is adopted.

For additional information and foundry guidelines on TC, the reader can refer to JEDEC JEP001-1A, as well as JSD47 and JESD22-A104.

Annex A (Informative) Bibliography

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